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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/694,891	10/29/2003	Yoshiyuki Shibata	60188-693	4097

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EXAMINER	
KENNEDY, JENNIFER M	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 07/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/694,891	SHIBATA, YOSHIYUKI	
	Examiner	Art Unit	
	Jennifer M. Kennedy	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *12 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) *4-12* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/29/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election of Claims 1-3 in the reply filed on May 12, 2004 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 3 are rejected under 35 U.S.C. 102(b) as being anticipated by Oowaki (U.S. Patent No. 4,825,268).

In re claim 1, Oowaki discloses a semiconductor device, comprising a first DRAM section including a first memory cell having a first capacitance (141, 13, 15) and a second DRAM section including a second memory cell having a second capacitance (142, 13, 15) different from the first capacitance, the first DRAM section (C1) and the second DRAM (C2) section being provided on the same semiconductor substrate (see specifically column 3, lines 20-60, column 4, lines 46-58, column 6, lines 16-35 and Figures 2 and 10).

In re claim 3, Oowaki discloses wherein a capacitor lower electrode of the first memory cell is provided in the semiconductor substrate (see Figure 10), whereas neither of a capacitor upper electrode and a capacitor lower electrode of the second memory cell is provided in the semiconductor substrate (see Figure 2, with column 6, lines 16-35). The examiner notes that Oowaki discloses that a trench and a planar capacitor may be formed on the same substrate. The examiner relies on the trench capacitor to be the capacitor wherein the lower electrode is formed in the substrate, whereas the planar capacitor of Figure 2 is being relied upon to show the capacitor that has neither the lower or upper electrode formed in the substrate.

Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Chang (U.S. Patent No. 5,814,547)

In re claim 1, Chang discloses a semiconductor device, comprising a first DRAM section including a first memory cell having a first capacitance and a second DRAM section including a second memory cell having a second capacitance different from the first capacitance, the first DRAM section and the second DRAM section being provided on the same semiconductor substrate (see column 3, lines 15-30 and Figure 11).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Oowaki (U.S. Patent No. 4,825,268) in view of applicant's admitted prior art ("AAPA" see specification pages 1-5 and Figures 12A-12C).

Oowaki discloses the device as claimed and rejected above, but does not disclose the method wherein the first DRAM section with lower capacitance has a higher operating voltage than that of the second DRAM section with higher capacitance. AAPA discloses that devices for use with portable terminals have a plurality of DRAM sections formed on the same semiconductor substrate have different operating voltages (see specification page 4) and conventional DRAM embedded LSI chips have a first DRAM section that needs to operate at high speed and a second DRAM section that is intended to operate at low power consumption with a sufficient signal holding characteristic (see specification, page 2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the first DRAM section with lower capacitance of Oowaki to operate at a higher operating voltage than that of higher capacitance second DRAM section in order to allow for a higher operating speed for first DRAM section because less charge is required to be moved, while allowing for a sufficient signal holding characteristic for the second DRAM section because of since a large amount of charge may be stored. The examiner notes the definition of the capacitance as defined in Merriam Webster's Collegiate Dictionary, Tenth edition, as the measure of the property that is equal to the ratio of the charge on either surface to the potential difference between the surfaces.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chang (U.S. Patent No. 5,814,547) in view of applicant's admitted prior art ("AAPA" see specification pages 1-5 and Figures 12A-12C).

Chang discloses the device as claimed and rejected above, but does not disclose the method wherein the first DRAM section with lower capacitance has a higher operating voltage than that of the second DRAM section with higher capacitance. AAPA discloses that devices for use with portable terminals have a plurality of DRAM sections formed on the same semiconductor substrate have different operating voltages (see specification page 4) and conventional DRAM embedded LSI chips have a first DRAM section that needs to operate at high speed and a second DRAM section that is intended to operate at low power consumption with a sufficient signal holding characteristic (see specification, page 2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the first DRAM section with lower capacitance of Chang to operate at a higher operating voltage than that of higher capacitance second DRAM section in order to allow for a higher operating speed for first DRAM section because less charge is required to be moved, while allowing for a sufficient signal holding characteristic for the second DRAM section because of since a large amount of charge may be stored. The examiner notes the definition of the capacitance as defined in Merriam Webster's Collegiate Dictionary, Tenth edition, as the measure of the property that is equal to the ratio of the charge on either surface to the potential difference between the surfaces.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Lee et al. (U.S. Patent Appl. 2003/0184953) discloses that the low and high capacitance capacitors on a substrate may be used to filtering high-frequency noises and form devices with high speed, respectively.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Kennedy whose telephone number is (571) 272-1672. The examiner can normally be reached on Mon.-Fri. 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (571) 272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Kennedy
Patent Examiner
Art Unit 2812